Dual Type-C interface PD Protocol dedicated SoC Chip CH9245

Version: 1.0

https://wch-ic.com

1. Overview

CH9245 is a dedicated SoC for dual Type-C interface PD protocol application, which can support PD protocol communication and power path management of 2 Type-C ports. CH9245 chip has built-in high-voltage LDOs with low static power consumption, high integration, streamlined peripherals, and firmware upgradable by using port C. CH9245F has a built-in USB2.0 signal 1/2 switching, which can be used for data communication switching between 2 Type-C ports. CH9245F has a built-in N-type MOSFET gate boost driver module, which can drive multiple high side NMOS for power path switching control. CH9245F chip also integrates a dual-channel differential OPA, which can be used for dual-port current detection.

The CH9245F can be widely used in various types of dual Type-C interfaces and related applications, such as portable displays, docking stations and multi-port cables.

2. Pinouts

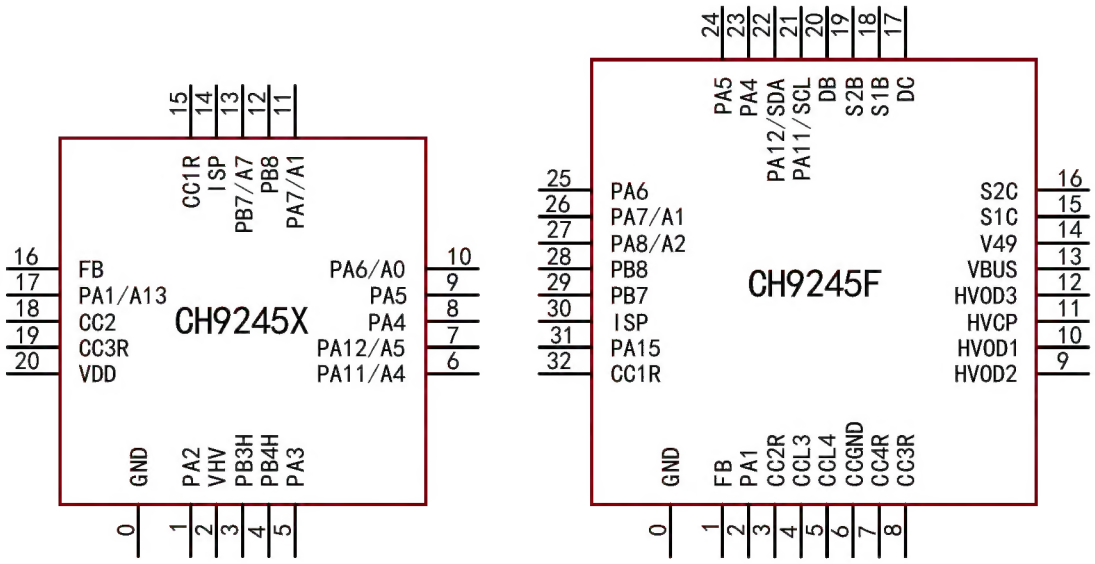


Table 2-1 Package Description

Package Form	Body Size	Pin Pitch		Package Description	Order Model
QFN20	3.0*3.0mm	0.4mm	15.7mil	Quad Flat No-lead Package	CH9245X
QFN32	4.0*4.0mm	0.4mm	15.7mil	Quad Flat No-lead Package	CH9245F

Note: Pin 0# is the EPAD of QFN20 or QFN32 package.

3. Pin Definitions

Table 3-1 Pin definitions

Pin No.		Pin name	Pin type[1]	Function description
CH9245X	CH9245F			
0	0	GND	P	Common ground
2	-	VHV	P	Working power supply input, externally connected with at least 1uF capacitance to ground.
20		VDD	P	Internal regulator LDO output, external 1uF capacitance to ground.
3		PB3H	I/O, HV	High voltage input and output pins powered by V_{HV}.
4		PB4H	I/O, HV	High voltage input and output pins powered by V_{HV}.
1		PA2	I/O, LV	General-purpose input and output pin.
5		PA3	I/O, LV	General-purpose input and output pin.
18		CC2	I/O/A	USB PD communication pin
16	1	FB	I/O/A	The input end of adjustable irrigation current is used for voltage feedback adjustment.
14	30	ISP	I/O/A	Positive input end of current detection module.
6	21	PA11/SCL	I/O/A	2-wire serial interface clock input, customized function.
7	22	PA12/SDA	I/O/A	2-wire serial interface data input and output, customized function.
8	23	PA4	I/O, LV	General-purpose input and output pin.
9	24	PA5	I/O, LV	General-purpose input and output pin.
10	25	PA6	I/O/A	General-purpose input and output pin.
11	26	PA7/A1	I/O/A	General-purpose input and output pin.
13	29	PB7	I/O/A	General-purpose input and output pin.
12	28	PB8	I/O	General-purpose input and output pin.
17	2	PA1	I/O/A	General-purpose input and output pin.
15	32	CC1R	I/O/A, Rd	USB PD communication pin
19	8	CC3R	I/O/A, Rd	USB PD communication pin
-	3	CC2R	I/O/A, Rd	USB PD communication pin
	7	CC4R	I/O/A, Rd	USB PD communication pin
	4	CCL3	I/O/A, LV	PD signal switch CC3R low voltage side port.
	5	CCL4	I/O/A, LV	PD signal switch CC4R low voltage side port.
	6	CCGND	P	Turn on the default Rd of CC3R and CC4R when grounded.
	13	VBUS	P, HV	Working power supply input, externally connected with 1uF capacitance to ground (pay attention to tolerant voltage).
	14	V49	P	Internal 4.9V regulator LDO output, external 1uF capacitor to ground.
	11	HVCP	O, HV	High voltage output of boost module.
	10	HVOD1	I/O, HV	NMOS for drive that high-side power path.
	9	HVOD2	I/O, HV	NMOS for drive that high-side power path.
	12	HVOD3	I/O, HV	NMOS for drive that high-side power path.

	20	DB	A	Input USB bus D+ data line.
	17	DC	A	Input USB bus D- data line.
	18	S1B	A	Output 1-terminal USB bus D+ data line.
	15	S1C	A	Output 1-terminal USB bus D- data line.
	19	S2B	A	Output 2-terminal USB bus D+ data line.
	16	S2C	A	Output 2-terminal USB bus D- data line.
	27	PA8/A2	I/O/A	General-purpose input and output pin.
	31	PA15	I/O	General-purpose input and output pin.

Note 1: Explanation of pin type abbreviations:

I = TTL/CMOS Schmidt input, which supports the input of VDD/V49 voltage range;

O = CMOS level 3-state output, which supports the output in the voltage range of VDD/V49;

P = power supply;

LV= low-voltage driving pin, which supports the input and output of VDD/V49 voltage range;

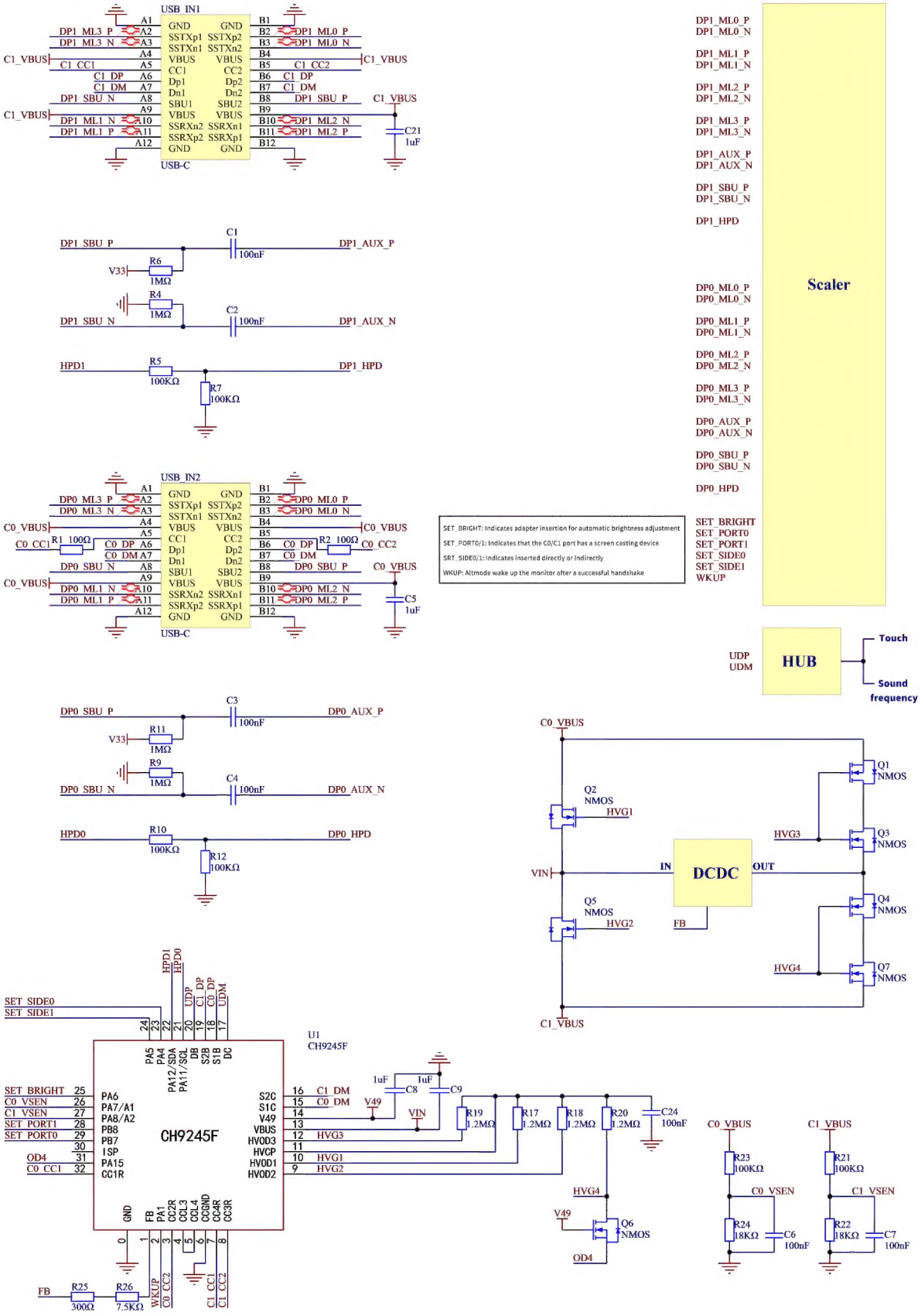
HV = high voltage driving pin, with VBUS rated at 4V ~ 28V, HVCP, HVOD1 and HVOD2 rated at 4V ~ 36V;

Rd = built-in controllable Rd pull-down resistor defined by Type-C specification, which can be used for PD power receiving end;

A= analog signal input or output, supporting VDD/V49 voltage range.

4. Reference Schematic Diagram

4.1 CH9245F, dual-port blind plug-in portable display screen scheme



5. Parameters

5.1 CH9245X Absolute Maximum

Critical or exceeding the absolute maximum value may cause the chip to operate improperly or even be damaged.

Name	Parameter description		Min.	Max.	Unit
T_A	Ambient temperature at work	Rated 5V or 9V, V_{HV} < 10V	-40	85	℃
		Rated 12V, V_{HV} ≥ 10V	-20	70	
T_J	Junction temperature range		-40	105	℃
T_S	Ambient temperature during storage		-40	125	℃
V_{HV}	External main supply voltage (V_{HV})		-0.3	14	V
V_{IN}	Input voltage on HV high voltage pins (PB3H, PB4H)		-0.3	V_{HV}+0.3	V
	Input voltage on other pins		-0.3	V_{DD}+0.3	V

5.2 CH9245F Absolute Maximum

Critical or exceeding the absolute maximum value may cause the chip to operate improperly or even be damaged.

Name	Parameter description	Min.	Max.	Unit
T_A	Ambient temperature at work	-40	85	℃
T_S	Ambient temperature during storage	-55	150	℃
V_{BUS}	Operating power supply voltage	-0.4	32.0	V
V_{49}	Supply voltage of pin V49	-0.4	6.5	V
H_{VCC}	Signal voltage of CC4R/CC3R pin	-0.4	32.0	V
V_{HVOD}	Signal voltage of HVOD1/HVOD2/HV0D3 pins	-0.4	40	V
V_{IOBC}	Signal voltage of DB/DC/S1B/S1C/S2B/S2C pins	-0.5	V_{49}+0.4	V

5.3 CH9245X Electrical Parameters (Test condition: T_A=25℃, V_{BUS}=5V~12V)

Name	Parameter description	Min.	Typ.	Max.	Unit
V_{HV}	Operating power supply voltage	4		12.6	V
V_{DD}	Internal regulator output, I/O voltage	4.7	4.8	4.9	V
I_{DD}	VDD external load capacity			15	mA
V_R	Voltage threshold for power-on reset of power supply	2.8	3.0	3.2	V
V_{OVP}	VHV threshold of OVP overvoltage reset	13.6	14.3	15	V
I_{HV}	Supply current in operation mode		5.5		mA
	Supply current in low power standby mode		64		uA

5.4 CH9245F Electrical Parameters (Test condition: T_A=25℃, V_{BUS}=5V~28V)

Name	Parameter description	Min.	Typ.	Max.	Unit
V_{BUS}	Supply voltage of VBUS pin	4.7	5~28	29	V
V_{49}	VDD49 pin LDO output voltage	4.7	4.9	5.1	V
V_{BUSOV}	Voltage threshold of VBUS overvoltage monitoring OVP	31.5	33	34.5	V
I_{CP}	Load current of HVCP booster module			60	uA
V_{IL}	Low-level input voltage of SCL/SDA pin	0		0.8	V

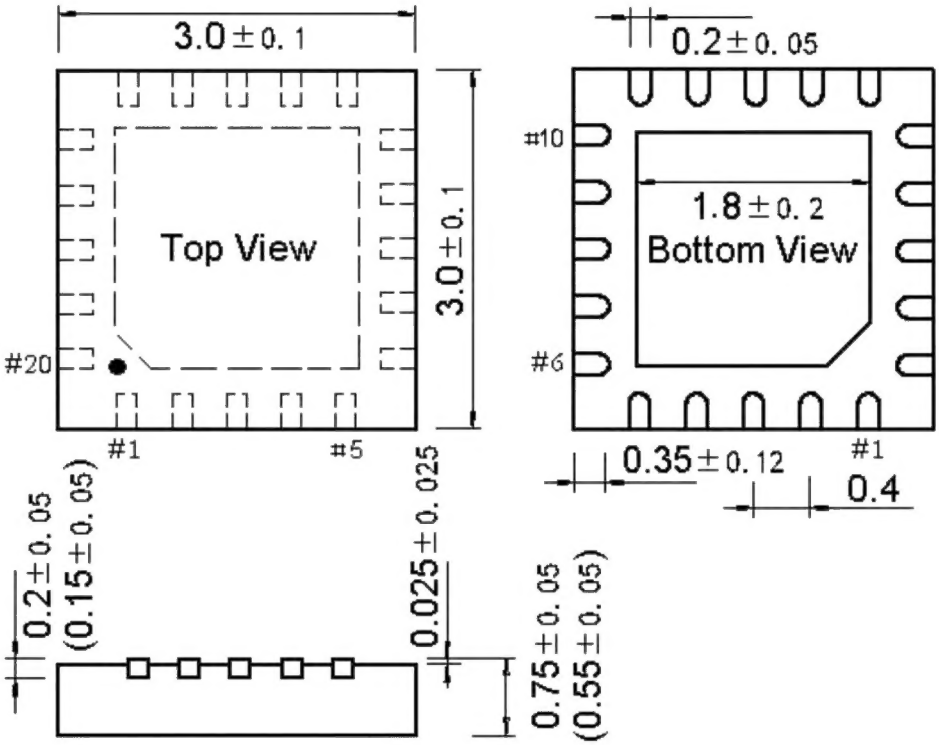
V_{IH}	High-level input voltage of SCL/SDA pin	2.1		5	V
T_{SD}	OTP over-temperature monitoring threshold	110	130	150	℃
V_R	Voltage threshold for power-on reset of power supply	2.8	3.0	3.2	V

6. Package Information

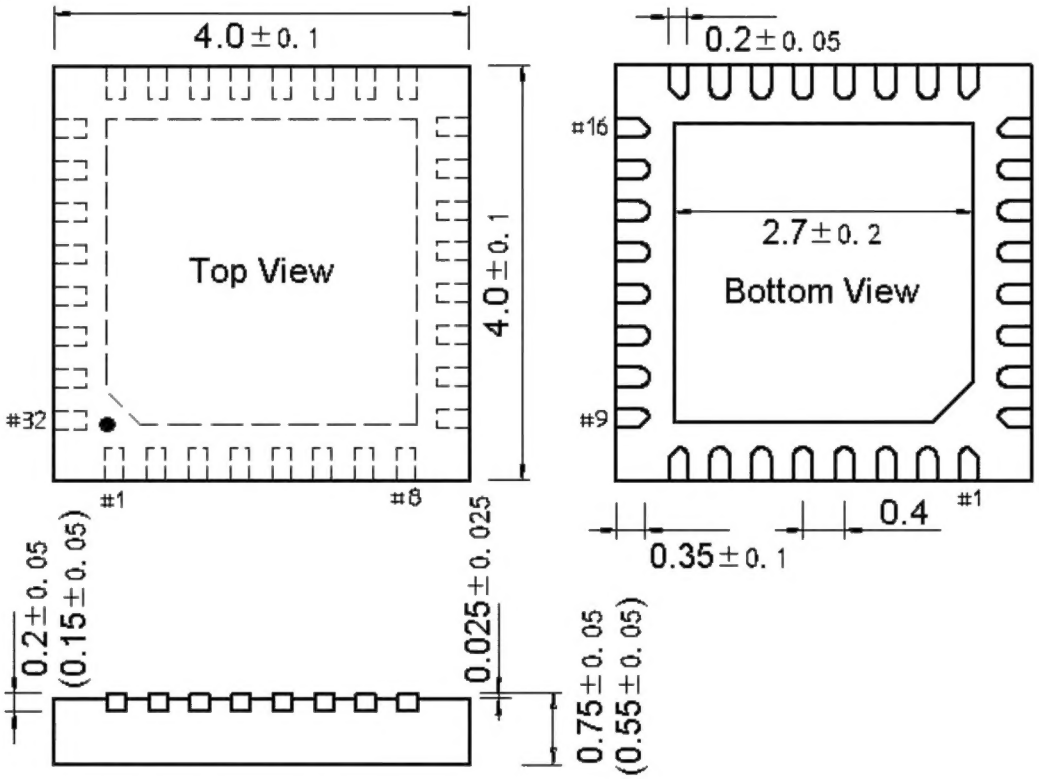
Note: All dimensions are in millimeters.

The pin center spacing values are nominal, without error. And the error of dimensions other than the pin center spacing values is not more than ±0.2mm.

6.1 QFN20



6.2 QFN32


4.0±0.1
Top View
4.0±0.1
#32
#1
#8
0.2±0.05
(0.15±0.05)
0.025±0.025
0.75±0.05
(0.55±0.05)
0.2±0.05
#16
2.7±0.2
Bottom View
#9
#1
0.4
0.35±0.1